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Abstract Of The Invention

A method of fabricating an integrated circuit having reduced threshold voltage shift is provided. A nonconducting region is formed on the semiconductor substrate and active regions are formed on the semiconductor substrate. The active regions are separated by the nonconducting region. A barrier layer and a dielectric layer are deposited over the nonconducting region and over the active regions. Heat is applied to the integrated circuit causing the barrier layer to anneal.

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